AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph [0001] beginning at page 1, line 4 , with the following rewritten paragraph:

--[0001] This application is a divisional of U.S. Patent Application No. 10/246,392 filed on 19 September 2002, and claims priority under 35 U.S.C. §119 from Korean Patent Application No. [2001-72590] 2002-2509, filed on [21 November 2001] 16 January 2002, the entirety of each of which is hereby incorporated by reference as if fully set forth herein.--

Page 6, replace paragraph [00015] with the following rewritten paragraph:

-- That is, in order to define the device active areas on the semiconductor substrate, the semiconductor substrate is partially [subsided] recessed to a predetermined depth and forming a trench, and a silicon insulating layer is filled in the trench. Then, a gate insulating layer is formed on the device active areas, and a gate conductive layer is formed on the gate insulating layer. A mask insulating layer is formed on the gate conductive layer. In this case, preferably, the gate conductive layer is conductive polysilicon such as an impurity doped polysilicon or polycide, which is combined with metal silicide, thereby improving the conductivity of the gate. Then, a gate pattern is formed on a mask insulating layer and a gate conductive layer through a photolithographic process, and an insulating layer for a sidewall spacer is formed on the sidewall of the gate pattern, thereby completing a gate process. Then, source and drain junctions are formed by an ion implantation method using the gate as a mask. Here, the insulating layer for the sidewall spacer is a silicon nitride layer, thereby increasing dry etch selectivity with a silicon oxide layer when a self-aligned

contact is formed. The source and drain areas form an N-type junction in the cell area, and form N-type and P-type junctions in the peripheral circuit area. A silicon insulating layer is formed, and a bit line conductive layer that is formed of polysilicon such as an impurity doped polysilicon and metal silicide, and a mask insulating layer for self-alignment that is formed of silicon nitride are formed on the silicon insulating layer. A bit line pattern is formed on the bit line conductive layer and the mask insulating layer for self-alignment, and then, an insulating layer spacer that is formed of silicon nitride is formed on the sidewall of the bit line pattern. In a case where the silicon insulating layer is formed, and the self-aligned contact is formed, the mask insulating layer and the insulating layer spacer that are formed of silicon nitride serve as a mask for dry etching.--

Page 20, replace paragraph [00049] with the following rewritten paragraph:

-- Referring to [FIG.8] FIGS. 7 and 8, a second ILD film 170 is thickly formed, and thereby step between the cell area C and the peripheral circuit area P is removed, and the surface of the semiconductor substrate 100 is planarized.--